Ultra Low Power Consumption IC for Green device

Tsukasa Fujimori

Keywords: Sensor network, Analog-Front-End Circuits, Analog-to-Digital Convertor, Digital Calibration Techniques

Abstract

The low power-consumption and highly accurate AFE LSI has been developed for sensor node. Proposed SAR ADC achieves both high effective resolution of 13 bits and extremely low power consumption of 3.0 mW, which is suitable for sensor network system.

Introduction

Energy saving technologies for CO2 emission reduction is becoming more and more important in recent years. Sensor network has been expected to be one of the most promising solutions for energy saving. However, large physical size and high power consumption of sensor nodes have been major constraints of its widespread usage.

Sensor nodes generally consist of batteries, wireless circuits, a microcomputer, sensors, and analog-front-end (AFE) circuits. Power consumption of sensors, wireless circuits and microcomputer in the sensor node can be reduced by adjusting measurement algorithms. However, it is difficult to reduce power consumption of the AFE circuits, which include amplifiers and analog-to-digital converters (ADCs), by adjusting measurement algorithms. Therefore, low-power AFE LSI is strongly required for sensor network.

Low-power AFE LSI

In order to reduce power consumption of the AFE LSI, it is effective to make supply voltage low with fine MOS transistors. However, when supply voltage is low, the operational margins of analog circuits decrease and it becomes difficult for analog circuits to keep their accuracy.

To expand the operational margins of AFE LSI at low supply voltage, we applied digital calibration techniques to the AFE LSI. Figure 1 shows the block diagram of developed AFE LSI. The AFE LSI consists of ADCs, a programmable gain amplifier (PGA), power supply circuits, and digital interface circuits. Two types of ADCs are implemented in AFE LSI; one is a successive-approximation-register (SAR) ADC with digital calibration techniques and the other is a delta-sigma ADC.

Fig. 2 shows a layout design of the AFE LSI. Fig. 3 shows a chip photograph of the AFE LSI. It was designed with the 0.13-micrometer CMOS process of TSMC. The chip size is 4 by 4 mm.

The simulation result of proposed ADCs is summarized in Table 1. The power consumption of SAR ADC is 3.0 mW and that of delta-sigma ADC is 5.8 mW. The area of SAR ADC and delta-sigma ADC is 1.6 mm2 and 1.0 mm2 respectively.

Average power consumption for 1 sample/sec of the AFE LSI using the SAR ADC is estimated at about 6 µW.

Conclusion

The low power-consumption and highly accurate AFE LSI has been developed for sensor node. Digital calibration techniques expand the operational margin of analog circuits at low supply voltage. As a result, proposed SAR ADC achieves both high effective resolution of 13 bits and extremely low power consumption of 3.0 mW, which is suitable for sensor network system.

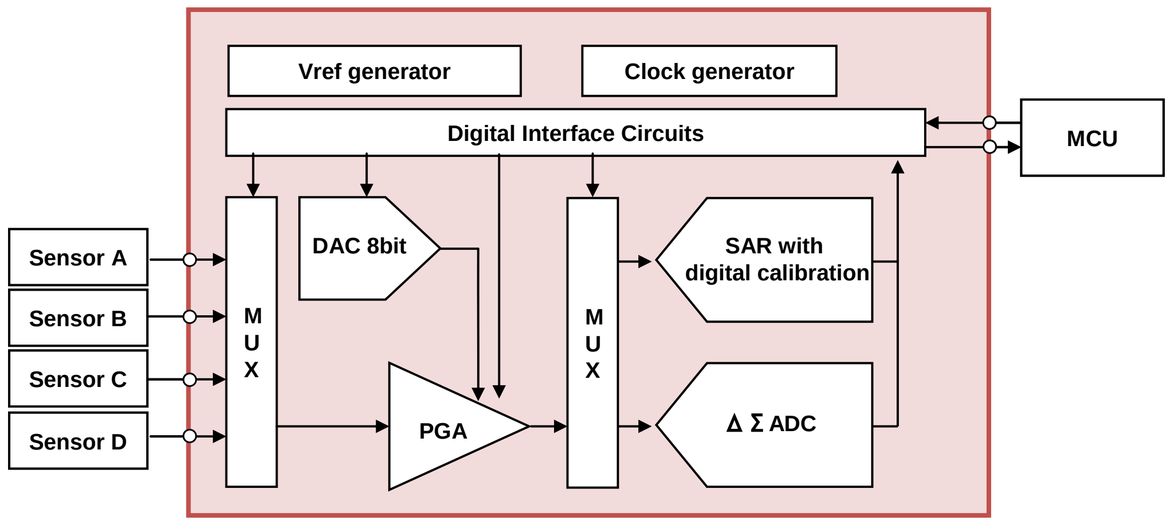

Fig. 1. Block diagram of AFE LSI

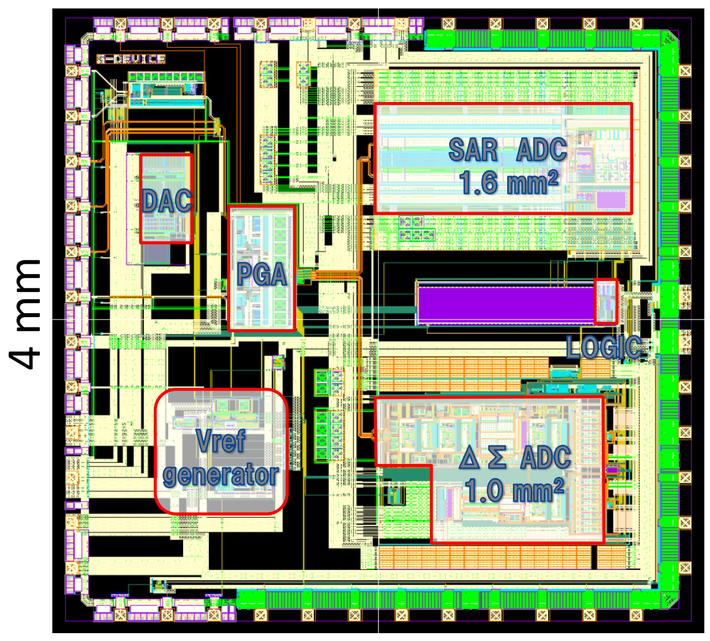

Fig. 2. Layout design of the AFE LSI.

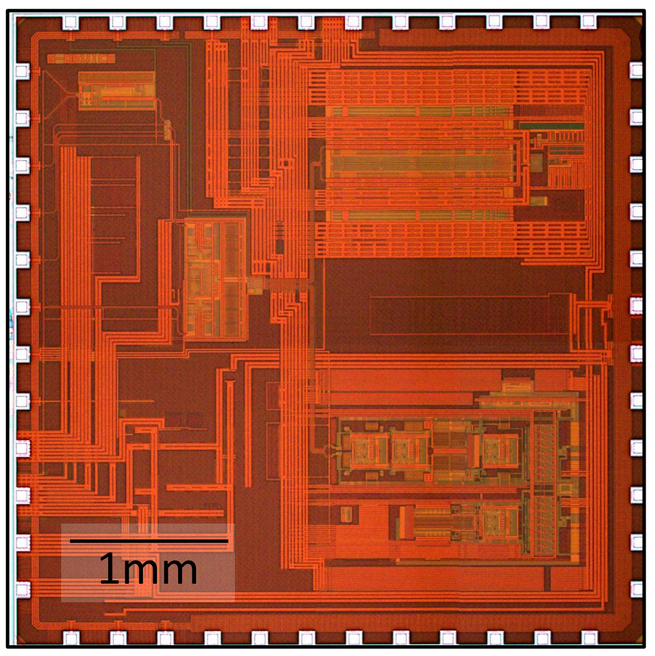

Fig. 3. Chip Photograph of the AFE LSI.
It was fabricated with 0.13-micrometer CMOS process.

Table 1. Simulation results of designed ADCs

Type	Power	Effective Resolution	Sample Rate	Chip Size
SAR	3.0 mW	13 bit	1 µs	1.6 mm²
ΔΣ	5.8 mW	14 bit	1 µs	1.0 mm²